formed in a source electrode formation scheduled region and a drain electrode formation scheduled region, respectively.

[0062] Next, as shown in FIG. **3**(C), the portion of the n-GaN layer **8**, which forms the source electrode **12** and the drain electrode **13**, is removed by the dry etching method using, for example, a chlorine based gas (for example, Cl_2 gas) or an inert gas.

[0063] Next, as shown in FIG. **3**(D), tantalum (Ta) **9** (for example, 10 nm in thickness), aluminum (Al) **10** (for example, 280 nm in thickness), and tantalum (Ta) **9** (for example, 10 nm in thickness) are evaporated in order.

[0064] Then, as shown in FIG. **3**(E), by removing the resists **15**A and **15**B using a removing liquid, the source electrode **12** and the drain electrode **13** having a Ta/Al/Ta stacked structure are formed.

[0065] After this, annealing is performed at temperatures below 600° C. (preferably, in the range of 530° C. to 570° C., or most preferably, 550° C.) in order to obtain the ohmic properties and thus the source electrode **12** and the drain electrode **13** as an ohmic electrode that come into ohmic contact with the n-AlGaN layer are formed. By performing annealing at such temperatures, the metal becomes more unlikely to condense and the electrode surface does not become coarse, and an excellent and flat surface can be obtained [refer to FIG. **4**(A) and FIG. **4**(B)].

[0066] Next, as shown in FIG. **3**(F) to FIG. **3**(H), a gate electrode is formed on the n-GaN layer **8** using the deposition lift-off method.

[0067] In other words, first, as shown in FIG. **3**(F), after resists (here, two layers) **15**C and **15**D are applied to the entire surface, patterning is performed so that an opening (its width is less than that of the n-GaN layer **8**; for example, 1 μm) is formed in a gate electrode formation scheduled region on the n-GaN layer **8**.

[0068] Next, as shown in FIG. **3**(G), nickel (Ni) **16** and gold (Au) **17** are evaporated in order. Then, as shown in FIG. **3**(H), by removing the resists **15**C and **15**D using a removing liquid, the gate electrode **5** having a Ni/Au stacked structure in which the nickel (Ni) layer **16** and the gold (Au) layer **17** are stacked.

[0069] After this, as shown in FIG. **3**(I), the SiN passivation film **4** is deposited and formed having a thickness of, for example, 10 nm on the entire surface using, for example, the chemical vapor deposition (CVD) method.

[0070] Then, as shown in FIG. **3**(J), part of the SiN passivation film **4** on the source electrode **12** and the drain electrode **13** is removed and a wire is provided so as to be connected to the source electrode **12** and the drain electrode **13**.

[0071] In this manner, the GaNFET as the semiconductor device according to the present embodiment is completed.

[0072] Therefore, according to the semiconductor device and its manufacturing method of the present invention, there is an advantage that reliability of an ohmic electrode in a high humidity environment can be improved while securing sufficient reliability of an ohmic electrode in a high temperature environment.

[0073] The present invention is not limited to the embodiment described above and there can be various modifications without departing from the concept of the present invention.

[0074] For example, in the embodiment described above, the semiconductor layer with which the source electrode **12** and the drain electrode **13** as an ohmic electrode come into contact is an n-type semiconductor layer, however, this is not limited and for example, an undoped semiconductor layer (that is, undoped GaN based semiconductor layer; undoped III-V group nitride compound semiconductor layer) may be used.

[0075] Further, in the embodiment described above, the configuration is such that the n-GaN layer **8** in the source electrode formation scheduled region and the drain electrode formation scheduled region is removed and there is no n-GaN layer **8** below the source electrode **12** and the drain electrode **13**, however, this is not limited.

[0076] For example, the n-GaN layer **8** in the source electrode formation scheduled region and the drain electrode formation scheduled region may be left thinly instead of being removed completely. In other words, there may be the n-GaN layer **8** below the source electrode **12** and the drain electrode **13**. In this case, the n-GaN layer **8** is thinner in thickness at a portion below the source electrode **12** and the drain electrode **13** than at a portion below the gate electrode **5**.

[0077] Further, for example, as well as the GaN layer **8** in the source electrode formation scheduled region and the drain electrode scheduled formation region, part of the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3**, which is below the GaN layer **8**, may also be removed. In this case, the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3** is thinner in thickness at a portion below the source electrode **12** and the drain electrode **13** than at a portion below the gate electrode **5**.

[0078] In the embodiment described above, explanation is given with a field effect transistor as an example, however, this is not limited, and the present invention can be applied widely to other semiconductor devices (in particular, a GaN based semiconductor device which is provided with an electrode in an n-type or an undoped semiconductor layer) such as a diode.

[0079] Further, in the embodiment described above, annealing is performed at predetermined temperatures (below 600° C.), however, this is not limited. For example, ion implantation or the like may be performed in the region [region immediately below the ohmic electrodes **12** and **13** in the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3**, which will be the backing layer of the ohmic electrodes **12** and **13** in the $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer **3**, so that the concentration (doping concentration; electron concentration) of the n-type impurity material in these regions is increased, thereby, obviating annealing for obtaining the ohmic properties.

[0080] In the embodiment described above, the n-GaN layer **8** is provided below the gate electrode **5**, however, this is not limited, and the present invention can be applied to a semiconductor device having no n-GaN layer.

What is claimed is:

1. A semiconductor device comprising:

a substrate;

an n-type semiconductor layer or an undoped semiconductor layer on the substrate; and

an ohmic electrode on the n-type semiconductor layer or the undoped semiconductor layer,

wherein said ohmic electrode comprises:

a tantalum layer formed on said n-type semiconductor layer or said undoped semiconductor layer;

an aluminum layer formed on said tantalum layer; and